WHAT IS CLAIMED IS:

1. An echo canceling system couplable between a transmit and receive path of a bit pump and adapted to receive and attenuate an echo in a receive signal propagating along said receive path, comprising:

a slave echo canceling stage configured to employ a filter coefficient to attenuate said echo;

a separation circuit, coupled to said slave echo canceling stage, configured to generate data representing a residual echo substantially exclusive of said receive signal; and

a master echo canceling stage, coupled to said separation circuit, configured to receive said data and modify said filter coefficient based thereon.

2. The echo canceling system as recited in Claim 1 wherein said master and slave echo canceling stages are configured to receive a transmit signal from said transmit path, said transmit signal being delayed to said master echo canceling stage.

3. The echo canceling system as recited in Claim 1 wherein said separation circuit comprises an equalizer/slicer stage configured to determine a symbol associated with said receive signal.

4. The echo canceling system as recited in Claim 3 wherein said separation circuit further comprises an estimator stage, coupled to said equalizer/slicer stage, configured to employ said symbol and develop an estimated receive signal.

5. The echo canceling system as recited in Claim 4 wherein master echo canceling stage is configured to generated an echo canceling signal and said separation circuit is configured to generate said data representing said residual echo as a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

6. The echo canceling system as recited in Claim 1 wherein said master and slave echo canceling stages each comprise finite impulse response filters and infinite impulse response filters.

7. The echo canceling system as recited in Claim 1 wherein said master and slave echo canceling stages each comprise a DC canceller.

8. For use with a bit pump having a transmit and receive path, a method of attenuating an echo in a receive signal propagating along said receive path, comprising:

employing a filter coefficient to attenuate said echo;

generating data representing a residual echo substantially exclusive of said receive signal; and

receiving said data and modifying said filter coefficient based thereon.

9. The method as recited in Claim 8 further comprising receiving a transmit signal from said transmit path.

10. The method as recited in Claim 8 wherein said generating comprises determining a symbol associated with said receive signal.

11. The method as recited in Claim 10 wherein said generating further comprises employing said symbol to develop an estimated receive signal.

12. The method as recited in Claim 11 further comprising generating an echo canceling signal and said generating said data representing said residual echo is a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

13. The method as recited in Claim 8 further comprising generating said filter coefficient.

14. The method as recited in Claim 8 wherein said modifying said filter coefficient is performed by finite impulse response filters and infinite impulse response filters.

15. A bit pump having a transmit and receive path, comprising:

a precoder, coupled to said transmit path, that preconditions a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, that reduces a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, that downsamples said receive signal propagating along said receive path; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal, including:

a slave echo canceling stage that employs a filter coefficient to attenuate said echo,

a separation circuit, coupled to said slave echo canceling stage, that generates data representing a residual echo substantially exclusive of said receive signal, and

a master echo canceling stage, coupled to said separation circuit, that receives said data and modifies said filter coefficient based thereon.

16. The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages receive said transmit signal, said transmit signal being delayed to said master echo canceling stage.

17. The bit pump as recited in Claim 15 wherein said separation circuit comprises an equalizer/slicer stage that determines a symbol associated with said receive signal.

18. The bit pump as recited in Claim 17 wherein said separation circuit further comprises an estimator stage, coupled to said equalizer/slicer stage, that employs said symbol and develops an estimated receive signal.

19. The bit pump as recited in Claim 18 wherein master echo canceling stage generates an echo canceling signal and said separation circuit generates said data representing said residual echo as a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

20. The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages each comprise finite impulse response filters and infinite impulse response filters.

21. The bit pump as recited in Claim 15 wherein said master and slave echo canceling stages each comprise a DC canceller.

22. A transceiver, comprising:

a framer that formats signals within said transceiver;

a bit pump coupled to said framer and having a transmit and receive path, including:

a precoder, coupled to said transmit path, that preconditions a transmit signal propagating along said transmit path;

a modulator, coupled to said precoder, that reduces a noise associated with said transmit signal;

an analog-to-digital converter, coupled to said receive path, that converts a receive signal received at said bit pump into a digital format;

a decimator, coupled to said analog-to-digital converter, that downsamples said receive signal propagating along said receive path; and

an echo canceling system, coupled between said transmit and receive path, that attenuates an echo in said receive signal, including:

a slave echo canceling stage that employs a filter coefficient to attenuate said echo,

a separation circuit, coupled to said slave echo canceling stage, that generates data representing a

residual echo substantially exclusive of said receive signal, and

a master echo canceling stage, coupled to said separation circuit, that receives said data and modifies said filter coefficient based thereon; and

a controller that controls an operation of said framer and said bit pump.

23. The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages receive said transmit signal, said transmit signal being delayed to said master echo canceling stage.

24. The transceiver as recited in Claim 22 wherein said separation circuit comprises an equalizer/slicer stage that determines a symbol associated with said receive signal.

25. The transceiver as recited in Claim 24 wherein said separation circuit further comprises an estimator stage, coupled to said equalizer/slicer stage, that employs said symbol and develops an estimated receive signal.

26. The transceiver as recited in Claim 25 wherein master echo canceling stage generates an echo canceling signal and said separation circuit generates said data representing said residual echo as a function of said estimated receive signal, said echo canceling signal and a delayed receive signal.

27. The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages each comprise finite impulse response filters and infinite impulse response filters.

28. The transceiver as recited in Claim 22 wherein said master and slave echo canceling stages each comprise a DC canceller.